LISTING OF THE CLAIMS

Please amend claims 1 and 5, and add new claim 15 as indicated below. This listing of claims replaces all prior versions

1. (Currently amended) Method for operating an array of nonvolatile charge trapping memory devices, comprising:

[[-]] before [[a]] block erasing the array ~~erase step of~~ by discharging substantially all of the non-volatile charge trapping memory devices of the array,

block programming the array by charging ~~of~~ substantially all of the non-volatile charge trapping memory devices of the array.

2. (Previously presented) Method according to claim 1, furthermore comprising after the erase operation programming some of the non-volatile memory devices of the array depending on data content to be stored in the non-volatile memory devices of the array.

3. (Previously presented) Method according to claim 2, furthermore comprising reading the data content stored in a non-volatile memory device of the array, wherein for reading the data content stored in a non-volatile memory device of the array at least one further non-volatile memory device having a dielectric charge trapping layer is used as reference cell which is programmed and erased for a block programming and block erase, respectively, of the non-volatile memory devices in the array.

4. (Previously presented) Method according to claim 3, wherein the memory devices of the array together function as reference cells.

5. (Currently amended) An electrical device comprising

an array of non-volatile charge trapping memory devices, ~~comprising:~~

[[-]] means for block programming the array by charging ~~of~~ substantially all of the non-volatile charge trapping memory devices of the array,

[[-]] means for block erasing the array by discharging ~~of~~ substantially all of the programmed non-volatile charge trapping memory devices of the array,

[[-]] control means for controlling the array of non-volatile charge trapping memory devices such that before block erasing of substantially all of the non-volatile memory devices of the array, substantially all of the non-volatile memory devices of the array are block programmed.

6. (Previously presented) An electrical device according to claim 5, wherein the non-volatile memory device comprises a transistor having a channel and a control gate, a dielectric charge trapping layer being located between the channel and the control gate.

7. (Previously presented) An electrical device according to claim 5, the array being provided with at least one non-volatile memory device for use as a reference cell in a sense amplifier.

8. (Previously presented) An electrical device according to claim 7, the array comprising means for programming and erasing the reference cell for a block-programming and block-erasing respectively of the non-volatile memory devices in the array.

9. (Previously presented) An electrical device according to claim 7, wherein the at least one reference cell is separate from the array.

10. (Previously presented) An electrical device according to claim 7, wherein the memory devices of the array together function as reference cells.

11. (Previously presented)) An electrical device according to claim 7, comprising means for comparing a read current from a non-volatile memory device in the array with a read current from the reference cell.

12. (Previously presented) An electrical device according to claim 7, comprising means for adapting a read current for reading the non-volatile memory devices in the array to the ageing of the reference cell.

13. (Previously presented) An electrical device according to claim 7, comprising means for adapting a required control gate voltage for reading the non-volatile memory devices in the array depending on the ageing of the reference cell.

14. (Previously presented)) An electrical device according to claim 5, wherein the array of non-volatile memory devices forms a non-volatile memory.

15. (New) A method according to claim 1, wherein the non-volatile memory devices of the array each include a dielectric charge trapping layer and wherein block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array includes trapping charge in the dielectric charge trapping layers.